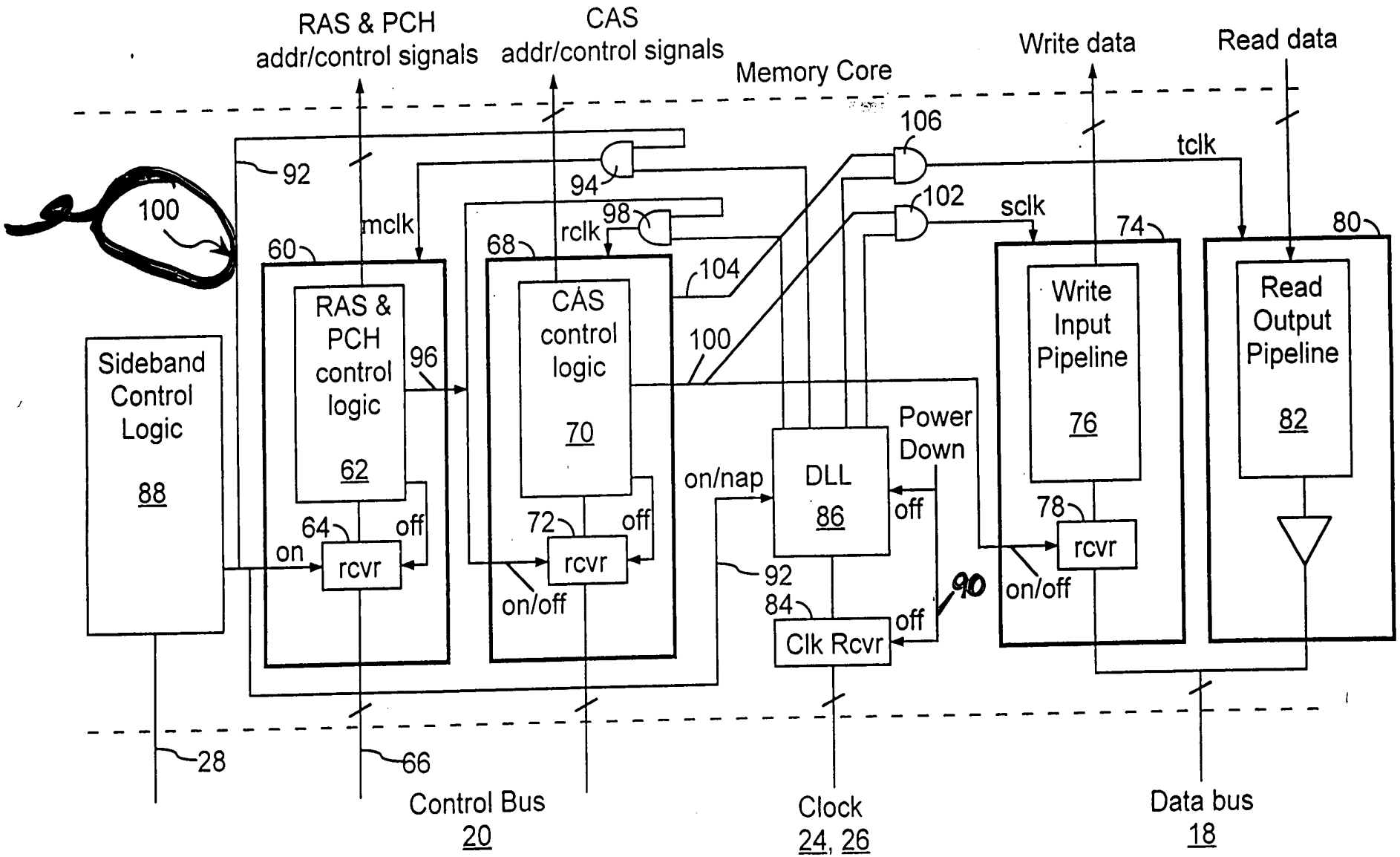
RAS & PCH
addr/control signals
CAS
addr/control signals
Memory Core
Write data
Read data
100
92
94
98
106
102
tclk
sclk
mclk
rclk
60
68
74
80
104
100
RAS &
PCH
control
logic
62
CAS
control
logic
70
Write
Input
Pipeline
76
Read
Output
Pipeline
82
Sideband
Control
Logic
88
96
Power
Down
on/nap
DLL
86
off
64
off
on
rcvr
72
off
rcvr
78
rcvr
on/off
on/off
92
90
84
off
Clk Rcvr
28
66
Control Bus
20
Clock
24, 26
Data bus
18

FIG. 5